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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,630	07/24/2003	Akiyoshi Tamura	L8462.03106	9060

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,630	TAMURA ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-14** are currently pending in this application is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on applications filed in JAPAN, 2002-309692 on 10/24/2002.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 07/24/2003 and made of record as Paper No. 091704. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1, 4, 5, 7, 10, 11, 13 and 14** are rejected under 35 U.S.C. 102(b) as being anticipated by Inata et al. (USP: 4,593,301 hereinafter referred to as "Inata").

Regarding claims **1 and 4**, Inata discloses in Fig. 7 and the corresponding texts as set forth in column 5, line 60-column 7, line 15, a heterojunction field effect transistor/a high electron mobility transistor (HEMT), comprises:

a semiconductor layer forming substrate formed with a plurality of semiconductor layers on a semi-insulative substrate/a semi-insulating GaAs substrate (11),

a gate electrode (20) formed on said semiconductor layer forming substrate,

N-type source area and drain area (17) formed by carrying out ion implantation to form N-type semiconductor on predetermined areas in said semiconductor layer forming substrate at both sides of said gate electrode, and by carrying out annealing process for activating the ion implanted areas,

an active layer/a GaAs channel layer (12A) including a predetermined semiconductor layer in said plurality of semiconductor layers between said source area and said drain area, and

an N-type carrier supply layer/an N-type AlGaAs (15) for supplying electron to said active layer formed of the upper or both of the upper and lower said semiconductor layers of said active layer between said source area and said drain area,

wherein at least one of the semiconductor layers to be said N-type carrier supply layer/the N-type AlGaAs is doped with Selenium (Se) (col. 6, lines 12-20) or Tellurium (Te).

It is noticed that the limitation "N-type source area and drain area formed by carrying out ion implantation to form N-type semiconductor on predetermined areas in said semiconductor layer forming substrate at both sides of said gate electrode, and by carrying out annealing process for activating the ion implanted areas" is taken to be a product by process limitation and consider non-limitation. In a product-by-process claim, it is the patentability of the claimed product and

not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972). Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ I S at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding claim **5**, Inata discloses in Fig. 7 and the corresponding texts as set forth in column 5, line 60-column 7, line 15, a heterojunction field effect transistor/a high electron mobility transistor (HEMT), comprises:

a semiconductor layer forming substrate formed with a plurality of semiconductor layers on a semi-insulative substrate/a semi-insulating GaAs substrate (11),

a gate electrode (20) formed on said semiconductor layer forming substrate,

N-type source area and drain area (17) formed by carrying out ion implantation to form N-type semiconductors on predetermined areas in said semiconductor layer forming substrate at both sides of said gate electrode and by carrying out annealing process for activating the ion

implanted areas, and

an N-type active layer/an N-type AlGaAs (15) formed of a predetermined semiconductor layer in said plurality of semiconductor layers between said source area and said drain area,

wherein the semiconductor layer to be said N-type active layer/the N-type AlGaAs is doped with Selenium (Se) (col. 6, lines 12-20) or Tellurium (Te).

Regarding claims **7 and 10**, Inata discloses in Fig. 7 and the corresponding texts as set forth in column 5, line 60-column 7, line 15, a manufacturing method of a heterojunction field effect transistor/a high electron mobility transistor (HEMT), comprises the steps of:

forming a semiconductor layer forming substrate having a plurality of semiconductor layers including at least a semiconductor layer, which serves as an active layer/a GaAs channel layer (12A), and a semiconductor layer at the upper side or at the both upper and lower sides of said active layer, which serves as an N-type carrier supply layer/an N-type AlGaAs (15) for supplying electron to said active layer, on a semi-insulative substrate/a semi-insulating GaAs substrate (11),

forming a gate electrode (20) on said semiconductor layer forming substrate, and

forming N-type source area (17) and drain area (17) by carrying out ion implantation for forming N-type semiconductors in predetermined areas of said semiconductor layer forming substrate at the both sides of said gate electrode and by carrying out annealing process for activating the ion implanted areas,

wherein, when forming said semiconductor layer forming substrate, at least one semiconductor layer to be said N-type carrier supply layer is doped with Selenium (Se) (col. 6, lines 12-20) or Tellurium (Te).

Regarding claim **11**, Inata discloses in Fig. 7 and the corresponding texts as set forth in column 5, line 60-column 7, line 15, a manufacturing method of a heterojunction field effect transistor/a high electron mobility transistor (HEMT), comprises the steps of:

forming a semiconductor layer forming substrate having a plurality of semiconductor layers including at least a semiconductor layer, which serves as an N-type active layer/an N-type AlGaAs (15), on a semi-insulative substrate/a semi-insulating GaAs substrate (11),

forming a gate electrode (20) on said semiconductor layer forming substrate, and

forming N-type source area (17) and drain area (17) by carrying out ion implantation for forming N-type semiconductors in predetermined areas of said semiconductor layer forming substrate at the both sides of said gate electrode and by carrying out annealing process for activating the ion implanted areas,

wherein, when forming said semiconductor layer forming substrate, said semiconductor layer to be said N-type active layer/the N-type AlGaAs is doped with Selenium (Se) (col. 6, lines 12-20) or Tellurium (Te).

Regarding claims **13 and 14**, Inata discloses the manufacturing method of a heterojunction field effect transistor/the high electron mobility transistor (HEMT) wherein annealing process carried out for forming said N-type source area and drain area is carried out in a manner of lamp annealing (col. 6, lines 12-20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **2-3, 6, 8-9, 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Inata et al. (USP: 4,593,301 hereinafter referred to as "Inata").

Inata discloses the claimed limitations except for the heterojunction field effect transistor wherein the active layer is an InGaAs layer and the N-type carrier supply layer is an InGaAs layer, wherein the semiconductor layer that serves as said N-type active layer is either one of InGaAs layer, GaAs layer and InP layer, wherein, when forming said semiconductor layer forming substrate, any one of InGaAs layer, GaAs layer and InP layer is formed as the semiconductor layer, which serves as said N-type active layer. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form an InGaAs layer as the active layer and the N-type carrier supply layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

09/17/04

Andy Huynh

Patent Examiner